



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,490	09/28/2001	Ko Miyazaki	501.40692X00	2765

20457 7590 09/21/2004

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-9889

EXAMINER

SHECHTMAN, SEAN P

ART UNIT

PAPER NUMBER

2125

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/964,490

Applicant(s)

MIYAZAKI ET AL.

Examiner

Sean P. Shechtman

Art Unit

2125

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 September 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
 - 2) ☐ Certified copies of the priority documents have been received in Application No. _____.
 - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2/20/03; 7/9/03
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims 1-25 are presented for examination.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered (See page 1, paragraph 2).

Drawings

4. Figures 10a-10d and 44-47 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (See page 8, paragraph 32 and page 13, paragraphs 66-69 of the instant specification). See MPEP § 608.02(g).
5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the menu for customer including a production type using a first photomask which has, as a blocker against an exposure light, an organic photosensitive resin, and a production type using a second photomask which has a metal film as a blocker against an exposure light, each upon exposure treatment must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

6. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Art Unit: 2125

Where applicable, the abstract should include the following:

- (1) if a machine or apparatus, its organization and operation;
- (2) if an article, its method of making;
- (3) if a chemical compound, its identity and use;
- (4) if a mixture, its ingredients;
- (5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

7. The abstract of the disclosure is objected to because it is not clear how the invention is directed toward a method of a method. Furthermore, it is not clear what is considered the fabrication step of the semiconductor integrated circuit device. Further still, it is not clear what is "depending on the fabrication step of the semiconductor integrated circuit device"- the method, the fabrication method, the use of a photomask, light blocking patterns made of metal, another photomask, light blocking patterns made of a resist film, or exposure treatment? Finally, it is not clear which method is referred to by "a method". Correction is required. See MPEP § 608.01(b).

8. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 1 recites the limitation "the production amount" in line 7. Claims 3 and 5 recite the limitation "the production amount" in at least line(s) 3. Claims 3 and 5 recite the limitation

Art Unit: 2125

"the threshold value" in the third paragraph(s). Claim 5 recites the limitation "the function of the semiconductor integrated circuit" in the third paragraph. Claim 10 recites the limitation "the constitution of a logic circuit" in line 6. Claim 11 recites the limitation "the constitution of a logic circuit" in line 6. Claim 14 recites the limitation "the optimum production type" in the last paragraph. Claim 16-17 recites the limitation "the using amount" in line 4. Claim 16-17 recites the limitation "the threshold value". Claim 20 recites the limitation "the stage". Claim 22 recites the limitation "the same data" in line 5. Claim 23 recites the limitation "the order of completion" in line 5. Claim 25 recites the limitation "the quality" in line 5. Claim 25 recites the limitation "the patterns" in line 5. There is insufficient antecedent basis for these limitation(s) in the claim(s).

10. Referring to claim 1, it is not clear what is required to be "depending on the production amount or fabrication step of the semiconductor integrated circuit device"- the method, the step, the use of a first photomask, a blocker against an exposure light, an organic material containing an organic photosensitive resin, a second photomask, a metal film?

11. Referring to claim 1, the phrase "the step of using" is not clear. Specifically, it is not clear if the step uses the second photomask or if the first photomask has, as a blocker against an exposure light, a second photomask which has a metal film.

12. Referring to claim 1, it is not clear if both the first and second photomasks are required to be used in the same step or more than one step.

13. Referring to claim 2, it is not clear how the method of claim 1 can comprise of more than one step if the method of claim one uses only "the step".

Art Unit: 2125

14. Referring to claim 2, it is not clear what is required to be “from the menu for customer”- a production type most suited for the semiconductor integrated circuit device or a production type most suited for the semiconductor integrated circuit device and a predetermined fabrication step of the semiconductor integrated circuit device?

15. Referring to claims 2 and 14, it is not clear if the semiconductor integrated circuit device has a predetermined fabrication step or if there is a predetermined fabrication step to fabricate the semiconductor integrated circuit device.

16. Referring to claim 4, the phrase “the step of using a photomask” is not clear. Specifically, it is not clear if the step of using a photomask is the same step of using a photomask as that described in claim 3, or another step.

17. Referring to claims 3-14 and 19-22, it is not clear what is required to be done “upon exposure treatment”- not exceeding threshold value, using a photomask, a blocker against exposure light, an organic material containing organic photosensitive resin film, a metal film, when the function has not been determined?

18. Referring to claim 6, it is not clear what is required to be done “in a stage”. Specifically, it is not clear if the metal film upon exposure treatment is in a stage or if the function of the semiconductor integrated circuit is determined in a stage or if the photomask is used in a stage.

19. Referring to claim 7, it is not clear what is required to be done “when the function of the semiconductor integrated circuit device has been determined” – exposure treatment, use of a photomask, a blocker?

Art Unit: 2125

20. Referring to claims 8, 9, 11, 13, and 21, it is not clear what is required to be done “prior to a mass production step”- using a photomask as a blocker against an exposure light, an organic material containing an organic photosensitive resin, exposure treatment?
21. Referring to claim 10, it is not clear what is required “in a step of forming patterns”- exposure treatment, using a first photomask, an organic material?
22. Referring to claims 10-13, it is not clear what is required in “using a second photomask”.
23. Referring to claim 11-13, it is not clear what is required “for forming patterns”.
24. Referring to claim 11, lines 9-13 are unclear. For example, what is done “upon exposure” or “in the mass production step”?
25. Referring to claim 14, it is not clear if the menu has a production type or if the photomask has a production type.
26. Referring to claim 14, line 9, it is not clear what is to be required by the phrase “each upon exposure treatment”.
27. Claim 16-17 requires “the photomask” in line 4, however, claim 15, from which claim 16 depends, requires a first and second photomask. Which photomask is “the photomask”?
28. Referring to claim 21, it is not clear what is required by the phrase “different each other”.
29. Examiner further invites the applicant’s attention to The MPEP 2173.05(a), which clearly states, in part:

“The meaning of every term used in a claim should be apparent from the prior art or from the specification and drawings at the time the application is filed. Applicants need not confine themselves to the terminology used in the prior art, but are required to make clear and precise the terms that are used to define the invention whereby the metes and bounds of the claimed invention can be ascertained.”

Art Unit: 2125

30. Due to the number of 35 USC § 112 rejections, the examiner has provided a number of examples of the claim deficiencies in the above rejections, however, the list of rejections may not be all inclusive. Applicant should refer to these rejections as examples of deficiencies and should make all the necessary corrections to eliminate the 35 USC § 112 problems and place the claims in proper format.

31. Due to the vagueness and a lack of clear definition of the terminology and phrases used in the specification and claims, the claims have been treated on their merits as best understood by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

32. Claims 1, 10, 18, 23, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 3,767,490 to Alberts.

Referring to claim 1, Alberts teaches a fabrication method of a semiconductor integrated circuit device (Col. 7, lines 13-14), comprising the step of using a first photomask which has, as a blocker against an exposure light, an organic material containing an organic photosensitive resin (Fig. 1, elements 14 or 16) and a second photomask which has, as a blocker against an exposure light, a metal film (Fig. 1, element 12), depending on the production amount or fabrication step of the semiconductor integrated circuit device (Col. 4, lines 38-64; Col. 3, lines 63-65). The examiner asserts that both layers are clearly blockers to exposed light. The

examiner asserts that exposing and developing in a conventional manner and according to conventional procedures meets the limitation "fabrication step of the semiconductor integrated circuit" or "depending on the... fabrication step of the semiconductor integrated circuit".

Referring to claim 10, Alberts teaches a fabrication method of a semiconductor integrated circuit device (Col. 7, lines 13-14), comprising the step of using a first photomask which has, as a blocker against an exposure light, an organic material containing an organic photosensitive resin upon exposure treatment in a step of forming patterns relating to the constitution of a logic circuit (Fig. 1, elements 14 or 16), while using a second photomask which has, as a blocker against an exposure light, a metal film upon exposure treatment in a step of forming patterns relating to a unit cell (Fig. 1, element 12).

Referring to claim 18, Alberts teaches a fabrication method of a semiconductor integrated circuit device (Col. 7, lines 13-14), comprising the steps of: (a) forming a first photomask having, as a blocker against an exposure light, an organic material containing an organic photosensitive resin on a semiconductor-integrated-circuit-device evaluator's side (Figs. 1-2, elements 16 or 14); (b) transferring a predetermined pattern onto a semiconductor wafer by exposure treatment with the first photomask, on a semiconductor-integrated-circuit-device maker's side (Figs. 1-2); and (c) evaluating the semiconductor wafer to which the predetermined pattern has been transferred, on the semiconductor-integrated-circuit-device evaluator's side (Col. 5, line 47 – Col. 6, line 15). The claims do not require that the evaluator be different from the maker nor do the claims require the evaluator be located separately from the maker. In an example, Alberts teaches evaluating contact holes (Col. 5, line 47 – Col. 6, line 15).

Referring to claim 23, Alberts teaches a fabrication method of a semiconductor integrated circuit device (Col. 7, lines 13-14), comprising the steps of: (a) disposing a semiconductor chip transfer region of a plurality of semiconductor integrated circuit devices on one photomask in the order of completion of a design period of the semiconductor integrated circuit devices (Col. 3, lines 51-65); and (b) carrying out exposure treatment with the one photomask (Fig. 1). A first layer is baked and completed and then a second layer is applied (Col. 3, lines 51-65) for fabricating integrated circuits (Col. 6, lines 56-58).

Referring to claim 24, Alberts teaches a fabrication method of a semiconductor integrated circuit device according to claim 23, wherein the one photomask has, as a blocker against an exposure light, an organic material containing an organic photosensitive resin (Col. 8, claim 6).

33. Claims 1, 3-7, 10, 12, 18, 23, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 5,776,836 to Sandhu.

Referring to claim 1, Sandhu teaches a fabrication method of a semiconductor integrated circuit device, comprising the step of using a first photomask which has, as a blocker against an exposure light, an organic material containing an organic photosensitive resin (Col. 5, lines 56-59) and a second photomask which has, as a blocker against an exposure light, a metal film (Col. 5, lines 62-67), depending on the production amount or fabrication step of the semiconductor integrated circuit device (Col. 4, line 50 – Col. 5, line 14).

Referring to claims 3 and 5, Sandhu teaches a fabrication method of a semiconductor integrated circuit device, comprising the steps of: (a) judging whether the production amount of the semiconductor integration circuit device exceeds a predetermined threshold production

amount or not; (b) when the production amount of the semiconductor integrated circuit device exceeds the threshold value, judging whether the function of the semiconductor integrated circuit device has been determined or not; (c) when the function has not been determined, using a photomask which has, as a blocker against an exposure light, an organic material containing an organic photosensitive resin film upon exposure treatment (Col. 7, lines 15-48).

Referring to claim 4, Sandhu teaches a fabrication method of a semiconductor integrated circuit device according to claim 3, further comprising the step of using a photomask which has, as a blocker against an exposure light, a metal film upon exposure treatment when the production amount of the semiconductor integrated circuit device is expanded to exceed the threshold value (Col. 5, lines 62-67).

Referring to claims 6, 7, 10, and 12, Sandhu teaches a fabrication method of a semiconductor integrated circuit device according to claim 5, further comprising the step of using a photomask which has, as a blocker against an exposure light, a metal film upon exposure treatment in a stage when the function of the semiconductor integrated circuit device is determined (Col. 5, lines 62-67).

Referring to claim 18, Sandhu teaches a fabrication method of a semiconductor integrated circuit device, comprising the steps of: (a) forming a first photomask having, as a blocker against an exposure light, an organic material containing an organic photosensitive resin on a semiconductor-integrated-circuit-device evaluator's side (Col. 5, lines 56-59); (b) transferring a predetermined pattern onto a semiconductor wafer by exposure treatment with the first photomask, on a semiconductor-integrated-circuit-device maker's side; and (c) evaluating the

Art Unit: 2125

semiconductor wafer to which the predetermined pattern has been transferred, on the semiconductor-integrated-circuit-device evaluator's side (Col. 7, lines 15-48).

Referring to claims 23 and 24, Sandu teaches a fabrication method of a semiconductor integrated circuit device, comprising the steps of: (a) disposing a semiconductor chip transfer region of a plurality of semiconductor integrated circuit devices on one photomask in the order of completion of a design period of the semiconductor integrated circuit devices; and (b) carrying out exposure treatment with the one photomask (Col. 4, line 50 – Col. 5, line 14).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

- (1). Determining the scope and contents of the prior art.
- (2). Ascertaining the differences between the prior art and the claims at issue.
- (3). Resolving the level of ordinary skill in the pertinent art.
- (4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

34. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 3,767,490 to Alberts in view of U.S. Pat. No. 4,000,054 to Marcantonio.

Referring to claim 8, Alberts teaches a fabrication method of a semiconductor integrated circuit device (Col. 7, lines 13-14), comprising the step of using a photomask (Col. 3, lines 39-66), as a blocker against an exposure light (Col. 3, lines 63-65), an organic material containing

Art Unit: 2125

an organic photosensitive resin upon exposure treatment (Fig. 1, element 14; Col. 8, claim 6; Col. 3, lines 1-6) prior to subsequent conventional procedures (Col. 3, lines 64-65) or prior to subsequent deposition or annealing (Col. 5, lines 39-41).

The examiner submits that the claims, as such, do not require that the method not be performed as a mass production step, as clearly set forth in claim 11. That is, the method could be interpreted as being performed as a mass production step prior to another mass production step (see the last paragraph of claim 11). The examiner respectfully submits that the claims, as such, do not even require that the mass production step be made on the semiconductor integrated circuit.

While Alberts teaches the method above, and Alberts teaches the method above prior to subsequent conventional procedures (Col. 3, lines 64-65) or prior to subsequent deposition or annealing (Col. 5, lines 39-41), Albert fails to teach that such subsequent conventional procedures or subsequent deposition or annealing are “a mass production step”.

However, Marcantonio teaches analogous art, wherein a depositing step is performed by batch processing or other mass-production techniques (Col. 7, lines 14-19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to modify the teachings of Alberts with the teachings of Marcantonio to perform deposition in “a mass production step”. One of ordinary skill in the art would have been motivated to combine these references because Marcantonio teaches mass production deposition with high reliability and at low cost (Col. 7, lines 6-14).

Art Unit: 2125

35. Claims 2 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,776,836 to Sandhu as applied to claims 1, 3-7, 10, 12, 18, 23, and 24 above, and further in view of U.S. Pat. No. 6,076,465 to Vacca.

Referring to claims 2 and 14, Sandhu teaches all of the limitations set forth above, but fails to teach a menu.

However, Vacca teaches analogous art, wherein a fabrication method of a semiconductor integrated circuit device, comprises: (a) a step wherein a maker prepares a menu for customer including a production type using a first photomask and a production type using a second photomask, and (b) a step wherein a production client selects a production type most suited for the semiconductor integrated circuit device or a predetermined fabrication step of the semiconductor integrated circuit device from the menu for customer (Col. 8, lines 48-54).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to modify the teachings of Sandhu with the teachings of Vacca. One of ordinary skill in the art would have been motivated to combine these references because Vacca teaches an automated photomask inspection system including a software program for determining the printability of a defect on a photomask onto a substrate, and determining which defects will effect the performance of a completed semiconductor device (Col. 1, lines 9-14; Col. 1, lines 57-65).

36. Claims 8, 9, 11, 13, and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,776,836 to Sandhu as applied to claims 1, 3-7, 10, 12, 18, 23, and 24 above, and further in view of U.S. Pat. No. 4,000,054 to Marcantonio.

Art Unit: 2125

Referring to claims 8, 9, 11, 13, and 19-22, Sandhu teaches a fabrication method of a semiconductor integrated circuit device, comprising the steps of: (a) using a first photomask having, as a blocker against an exposure light, an organic material containing an organic photosensitive resin upon exposure treatment for forming patterns relating to the constitution of a logic circuit of the semiconductor integrated circuit device, (b) using a second photomask having a metal as a blocker against an exposure light upon exposure treatment for forming patterns relating the constitution of the logic circuit in the mass production step of the semiconductor integrated circuit device, and (c) using the second photomask having a metal as a blocker against an exposure light upon exposure treatment for forming patterns relating to a unit cell prior to the mass production step (Col. 4, line 50 – Col. 5, line 14).

Referring to claims 8, 9, 11, 13, and 19-22, Sandhu teaches all of the limitations set forth above, but fails performing a step or steps before or in a mass production step.

However, Marcantonio teaches analogous art, wherein steps are performed before or by batch processing or other mass-production techniques (Col. 7, lines 14-19).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to modify the teachings of Sandhu with the teachings of Marcantonio to perform before or by “a mass production step”. One of ordinary skill in the art would have been motivated to combine these references because Marcantonio teaches mass production deposition with high reliability and at low cost (Col. 7, lines 6-14).

Art Unit: 2125

37. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,776,836 to Sandhu as applied to claims 1, 3-7, 10, 12, 18, 23, and 24 above, and further in view of U.S. Pat. No. 6,211,013 to Park.

Referring to claim 15, Sandhu teaches a fabrication method of a semiconductor integrated circuit device, comprising, upon forming patterns of the semiconductor integrated circuit device, properly using (a) exposure treatment using a first photomask having, as a blocker against an exposure light, an organic material containing an organic photosensitive resin; (b) another exposure treatment using a second photomask having a metal film as a blocker against an exposure light. Referring to claim 16, Sandhu teaches a fabrication method of a semiconductor integrated circuit device according to claim 15, comprising the steps of: judging whether the using amount of the photomask exceeds a predetermined threshold using amount or not; judging whether the first photomask is usable or not when the using amount of the photomask is less than the threshold value, and carrying out exposure treatment with the first photomask when the first photomask is usable. Referring to claim 17, Sandhu teaches a fabrication method of a semiconductor integrated circuit device according to claim 15, comprising the steps of: judging whether the using amount of the photomask exceeds a predetermined threshold using amount or not; judging whether the second photomask is usable or not when the using amount of the photomask exceeds the threshold value, carrying out exposure treatment with the second photomask when the second photomask is usable, judging whether the first photomask is usable or not when the second photomask is unusable, carrying out exposure treatment with the first photomask when the first photomask is usable (Col. 4, line 50 – Col. 5, line 14).

Art Unit: 2125

Referring to claims 15-17, Sandhu teaches all of the limitations set forth above, but fails teach direct writing using e-beam.

However, Park teaches analogous art, including direct writing treatment using an energy beam (Col. 6, claim 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to modify the teachings of Sandhu with the teachings of Park. One of ordinary skill in the art would have been motivated to combine these references because Park teaches advantageously using e-beam lithography to obtain smaller line width gap, thereby reducing a size of an electrically formed quantum dot down to a few tens of nanometers (Col. 3, lines 37-52).

38. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 5,776,836 to Sandhu as applied to claims 1, 3-7, 10, 12, 18, 23, and 24 above, and further in view of U.S. Pat. No. 5,965,306 to Mansfield.

Referring to claim 25, Sandhu teaches a fabrication method of a semiconductor integrated circuit device, comprising the steps of: (a) in step, carrying out exposure treatment using a photomask having, disposed thereon, a semiconductor chip transfer region of a plurality of semiconductor integrated circuit devices and judging the quality of the patterns thus transferred; and (b) in a second step, carrying out another exposure treatment using a photomask having, disposed thereon, a semiconductor chip transfer region of the plurality of semiconductor integrated circuit devices which are judged bad in said first step and judging quality of the

Art Unit: 2125

patterns thus transferred, wherein the photomasks used in the first and second steps each has, as a blocker against an exposure light, an organic material containing an organic photosensitive resin.

Referring to claim 25, Sandhu teaches all of the limitations set forth above, but fails teach that said steps are pre-production steps.

However, Mansfield teaches analogous art, wherein pre-production steps carrying out exposure treatments using photomasks (Col. 7, lines 41-65).

Therefore, it would have been obvious to one of ordinary skill in the art at the time that the invention was made to modify the teachings of Sandhu with the teachings of Mansfield. One of ordinary skill in the art would have been motivated to combine these references because Mansfield teaches pre-production steps increased mask yields, improved turn-around-time, and reduce mask costs (Col. 4, lines 49-64).

Conclusion

39. The prior art or art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents or publications are cited to further show the state of the art with respect to advantages of performing mass-production.

U.S. Pat. No. 4,313,254 to Feldman.

40. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean P. Shechtman whose telephone number is (703) 305-7798.

The examiner can normally be reached on 9:30am-6:00pm, M-F.

Art Unit: 2125

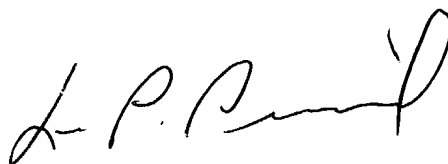
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on (703) 308-0538. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SPS

Sean P. Shechtman

September 15, 2004

A handwritten signature in black ink, appearing to read 'L. P. Picard', with a stylized flourish at the end.

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100